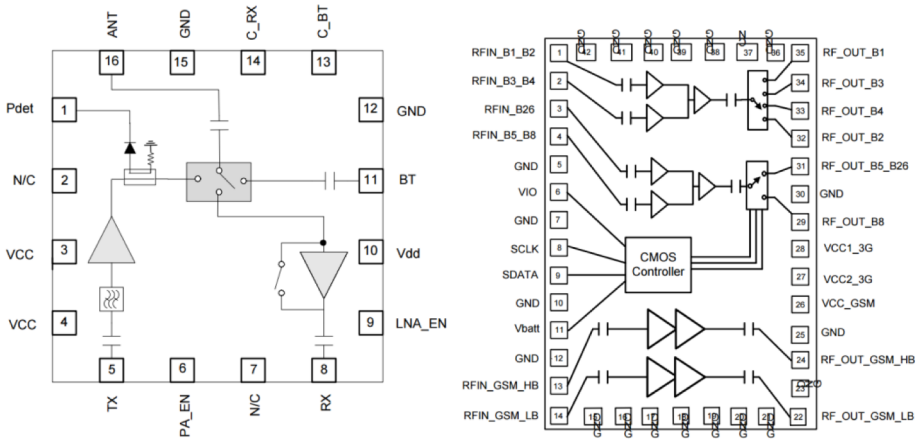
Bridging the Gap Between RF Front-End Module Characterization and Production Test With the Semiconductor Test System

The rapid evolution of wireless connectivity has driven continual consumer thirst for more data throughput and reduced time to market. These pressures have led to modern signaling standards such as 802.11ac and LTE-Advanced, which have placed even more challenging design and test requirements on the most nonlinear and energy-demanding component in the transmitter, the RF power amplifier. The industry trend to shorten time to market is to decrease system complexity by integrating transmitter and receiver functionality into a single front-end module (FEM) and integrating multiple communication standards into a multiband, multimode power amplifier (MMPA). Figure 1 shows examples of these devices in today's market where product quality is paramount and tests for such highly integrated and high-performance devices include many challenges. This white paper highlights some test challenges and explains how NI PXI instrumentation addresses them with the same hardware and software platform in both characterization and production test environments.



(a) (b)

Figure 1. *Example of (a) FEM and (b) MMPA*

Characterization and Production Goals

To fully understand a device's performance, characterization test engineers validate its design during normal conditions, corner cases, and harsh environments. Because of the exhaustive set of test requirements, characterization is typically performed on a small batch of devices. Conversely, production test engineers ensure the device is manufactured to the design specification at very high volumes while closely monitoring test throughput and yield. Although characterization test plans often call for testing under advanced conditions, such as high temperature or with a dynamic power supply, production engineers may decide to avoid such conditions to reduce test time, especially if performance can be *guaranteed by design*. Both characterization and product test engineers care about test speed, but for different reasons. Faster test speed leads to more test coverage on the small batch for characterization, whereas this leads to increased throughput for production. Traditionally, optimizing for speed meant sacrificing measurement quality, thus characterization and production often opted for different instrumentation. When introducing a new product, there is extensive effort to ensure measured performance in production agrees with measured performance in characterization. This data correlation effort can often uncover issues with the device under test (DUT), test methods, differences in equipment used, and assumptions of operation, which often increase the time to market for a new product.

These are just a few differences in the characterization and production test activities. However, there are many measurements performed in both activities. For example, adjacent channel power ratio (ACPR) and error vector magnitude (EVM) are often performed in both characterization and production. If a single piece of equipment can meet both the characterization and production requirements with a speed, quality, and price acceptable to both organizations, the hand-off to production is smoother. Maximizing commonality for both activities significantly reduces the time to market for a new product.

Bridging the Gap Between Characterization and Production

The NI approach shares a common hardware and software platform to bridge this gap and reduce size, cost, and time to market. Many instruments designed solely for production tend to be built on a proprietary interface with fixed functionality; thus, as new requirements emerge, the production test engineer is left to either get creative, wait, or buy a whole new platform. The PXI platform is an open industry standard on which NI builds all of its test systems. With a modular, open platform, both characterization and production engineers can benefit from module-level upgrades to instrumentation and computer technology as test requirements evolve. Computational performance is a key driver for test speed as many complex RF measurements involve significant signal processing analysis. Therefore, the ability to simply increase test speed by upgrading the processor with no other changes is extremely beneficial.

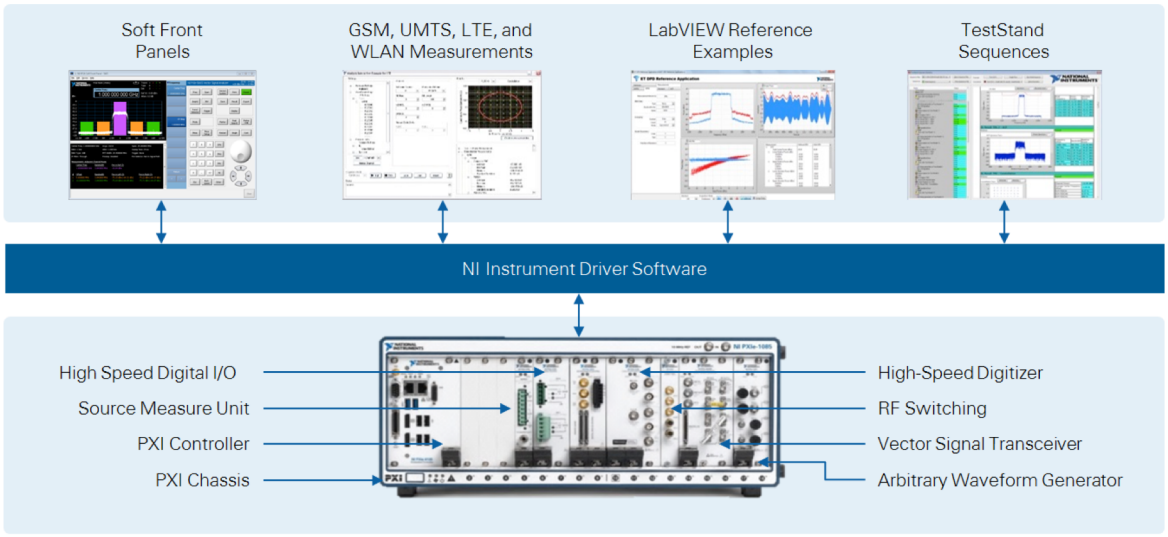


Figure 2. *Common System Configuration for RF FEM Characterization*

Testing RF FEMs requires not only RF instruments but also non-RF instruments such as arbitrary waveform generators (ARBs), source measure units (SMUs), high-speed digital with per pin measurement units (PPMUs), oscilloscopes (O-scopes), and digital multimeters (DMMs). In addition to instrumentation, signal switching and coprocessing capabilities are often required or used to enhance testing. NI offers all these capabilities in PXI with various performance options for each. Instrumentation hardware is nothing without software. Software is the critical piece for measurement algorithms and automation. NI provides the tools to accelerate productivity and performance for both production and characterization test engineers. Figure 2 illustrates a common test system used for RF FEM characterization; these are the same hardware and software modules used for production applications.

Device Interfacing Characterization and Production

Characterization test stations often use PXI instrumentation interfacing directly with cables and limited fixtures to a single DUT; production test stations frequently interface with multiple DUTs/sites at a time. Although characterization test stations tend to be static for a long time, production test cells may be reconfigured weekly or even daily as product shipping needs require. In production, the PXI platform can be racked and cabled if rapid reconfigurability is not required and the user can take on the task of system integration, fixture calibration, and

development. This use case is common in industry and accepted by many OEM device manufacturers looking to minimize capital equipment cost for a highly specialized tester. For many production users, however, there are practical requirements needed above the PXI platform to meet what the mainstream user expects such as a standard load-board interface, hard dock mechanics, chip handler integration, DUT-centric programming, multisite abstraction, standard test data format (STDF) reports, and an integrated multiport RF subsystem. Although PXI is the common core for the NI approach to semiconductor test, the Semiconductor Test System (STS) augments this platform to add features needed by many mainstream production test engineers.

Figure 3. *The STS Series (From Left to Right, STS-T2, STS-T1, STS-T4)*

Introduction to the Semiconductor Test System

The STS is a PXI-based alternative to traditional automated test equipment (ATE) for high-volume semiconductor production test. It combines the NI PXI platform, TestStand test management software, and LabVIEW graphical programming inside a fully enclosed test head. The STS enclosure houses all the key components of a production tester including system controllers; DC, digital, analog, and RF instrumentation; DUT interfacing; and device handler/prober docking mechanics. The compact design of the STS eliminates the extra floor space, power, and maintenance required by traditional ATE testers that unnecessarily increase the cost of test. Additionally, engineers can take advantage of the open, modular STS design to use the latest industry-standard PXI modules for more instrumentation and computing power. NI combines the technical capabilities of the STS with services and support to deliver an overall lower cost solution to RFIC production test.

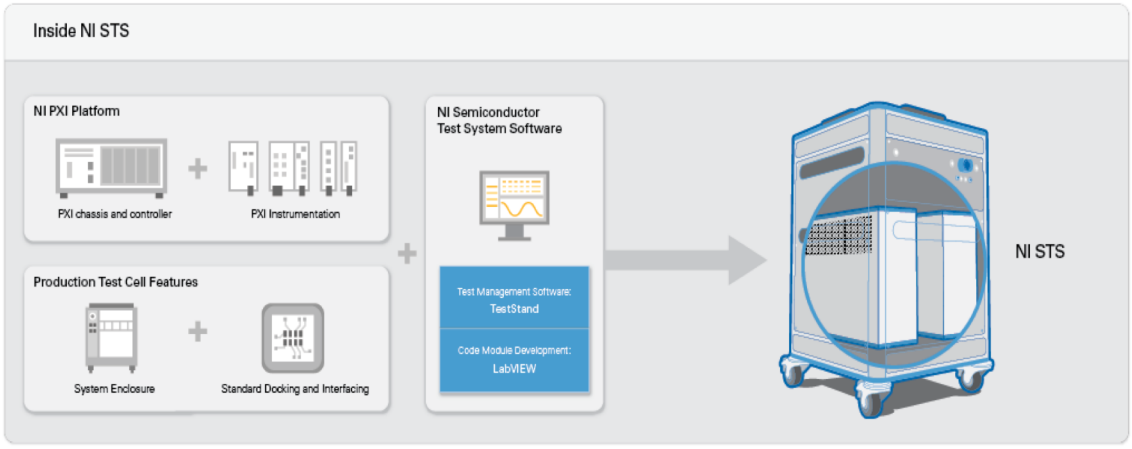


Figure 4. *STS High-Level Components*

Tester Size Options

The STS is available in three test head sizes, from the T1 with one PXI chassis to the T4 with four PXI chassis. All three STS sizes include common docking and tester I/O interfaces. Based on the size and cost of the T1, and the performance of PXI instruments, engineers can economically deploy either a T1 tester or a stand-alone PXI system in characterization. This gives engineers the ability to use identical hardware and software for both characterization and production test, resulting in easier correlation of data and ultimately shorter time to market.

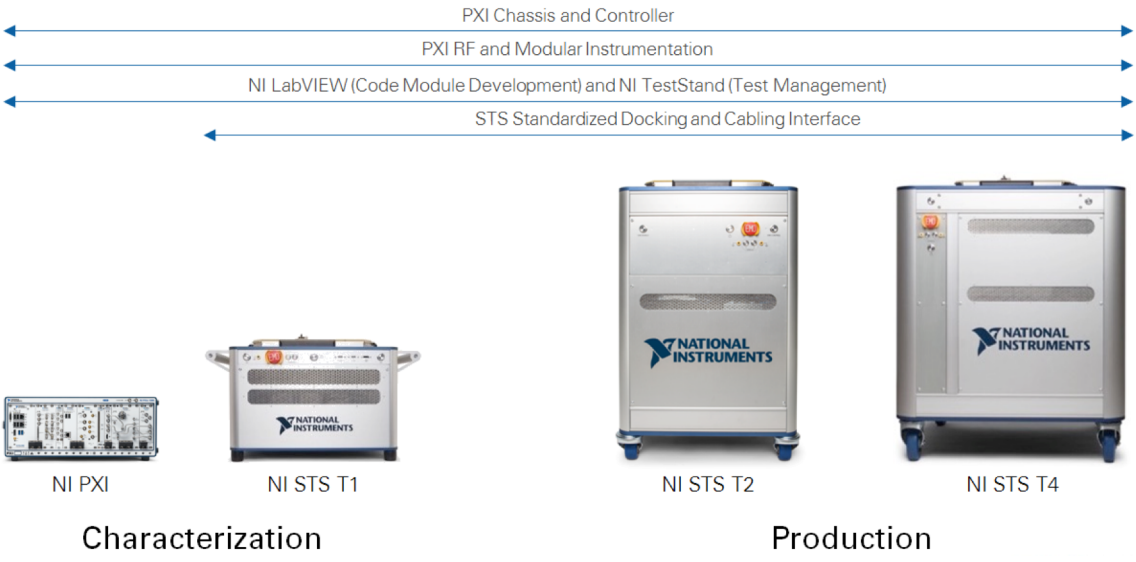


Figure 5. *The STS for Characterization and Production*

RF Measurement Capabilities

The STS provides a fully integrated RF test capability for both wireless standards and general-purpose RF measurements. The core RF measurement algorithm base for the STS is established on the NI-RFmx measurement software suite. NI-RFmx is a measurement-focused software suite for high-performance and easy-to-use measurements with NI RF instrumentation. Below is a list of key modulation formats and measurements supported with NI RF instrumentation.

Supported Modulation Formats

- Cellular Standards
  - LTE/LTE-Advanced
  - WCDMA/HSPA+
  - TDSCMDA
  - CDMA2K
  - EVDO
  - GSM/EDGE/EDGE+
- Wireless Connectivity Standards
  - 802.11a, b, g, n, ac, ah, af, and so on
  - Bluetooth, BT-LE
- Nonstandard
  - FM, AM, FSK, BPSK, QAM (16 to 4,096)

Supported Measurements

- Error Vector Magnitude (EVM)
- Spectral Emissions Mask (SEM)
- Adjacent Channel Power Ratio (ACPR)
- Output RF Spectrum (ORFS)
- Power Versus Time (PVT)
- Third-Order Intercept (TOI)
- Noise Figure (NF)
- Digital Predistortion (DPD)
- Dynamic Power Supply (DPS)/Envelope Tracking (ET)
- Spurious Response/Harmonics
- S-Parameter, up to 48 Ports (Using NI-5530 RF Subsystem)
- Power—Including Fast Power Servo With FPGA
- Custom—RAW IQ Fetch

RF Measurement IO

Vector Signal Transceiver

The core of the RF test instrument inside the STS is the PXIe-5646R vector signal transceiver (VST), which includes an RF vector signal generator and vector signal analyzer in a single 3-slot PXI module connected to a user-programmable FPGA. The VST supports frequencies up to 6 GHz with 200 MHz of instantaneous generation and analysis bandwidth. Because the VST is enabled by LabVIEW reconfigurable I/O (FPGA), this opens the possibilities for many innovative test speed acceleration techniques such as fast power servo. Figure 6 shows a conceptual diagram of this capability available inside the STS and with stand-alone PXI stations. By doing power servo in hardware, users can reduce this operation sometimes by an order of magnitude. As shown in Figure 2, the VST combined with NI-RFmx measurement software is the common piece for both production and characterization test on the PXI test platform.

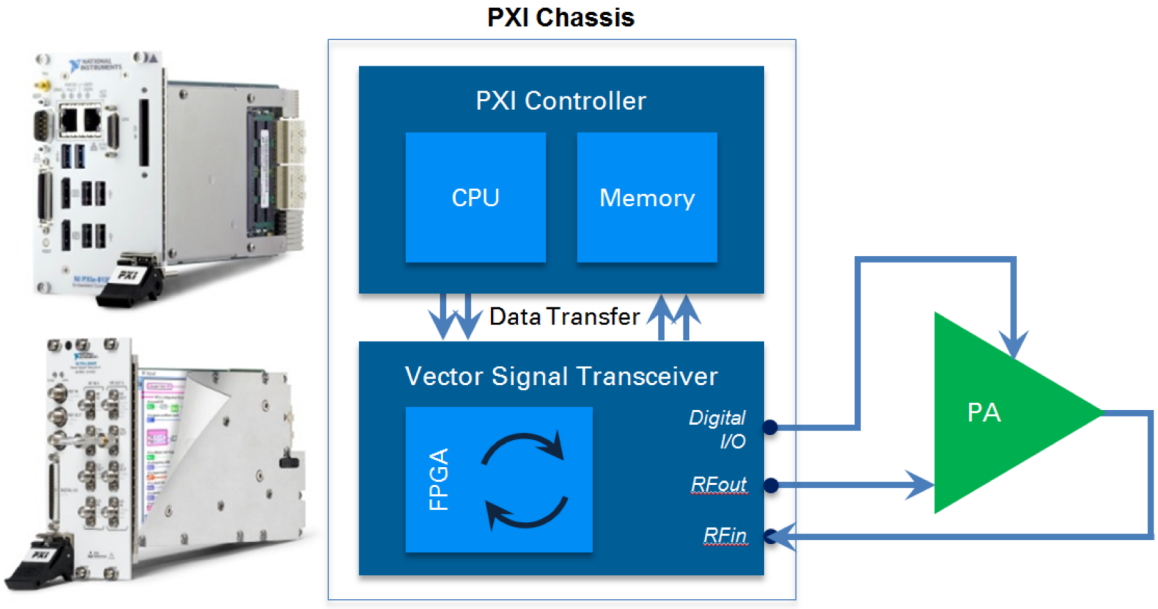


Figure 6. *PXIe-5646R VST Hardware Amplifier Servo Concept*

The STS RF Subsystem

Production test engineers need a flexible and robust switching solution to perform multisite test on multiport RF devices. Many test plans call for S-parameter and modulation measurements on all RF ports of a device. For these reasons, the STS includes a fully integrated RF subsystem enabling the following capabilities:

- Up to 48 bidirectional RF ports at the tester I/O interface
- Up to 4 parallel VSTs
- Full vector S-parameter measurements across all 48 ports (per port couplers)
- Per port low-noise amplifier (LNA)
- System-level vector and scalar calibration
- RF blind mate interface

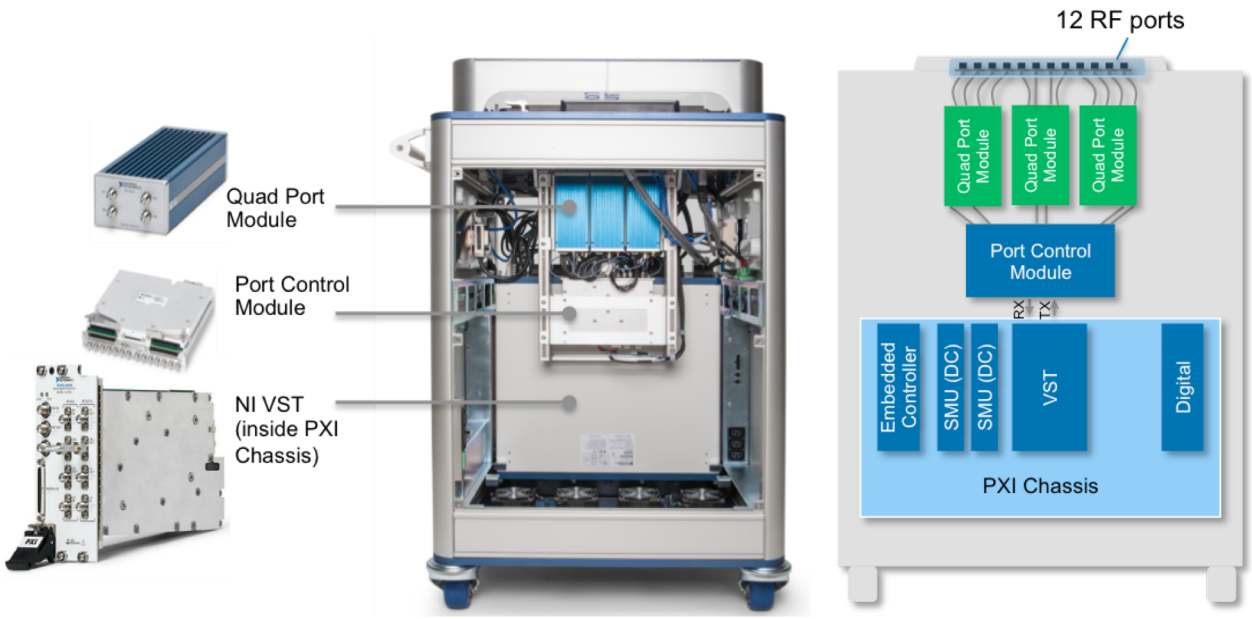


Figure 7. *The STS RF Subsystem (Side Panel Off Tester)*

The STS RF subsystem is a modular and flexible architecture that gives users the ability to configure a tester to scale to their parallelism target, port counts, and cost per port requirements. The STS RF subsystem can be configured from 12 to 48 ports with one to four parallel subsystems. Common system resources and configurations are shown in the table below.

STS System Configuration

Common System Resources for RFIC Testing in STS	
RF Subsystem	• STS T1: Up to 12 RF ports with one VST • STS T2: Up to 24 RF ports with two VSTs • STS T4: Up to 48 RF ports with four VSTs
DC Source Measure (SMUs)	• Precision system SMU (up to 24 channels per system) • 4-channel SMU (up to 96 channels per system)
Digital Instruments	• Up to 200 MHz with PPMU (up to 240 channels)
Optional Instruments	• Digitizers/oscilloscopes • Arbitrary waveform generators • Dynamic signal acquisition instruments • Power supplies • High-speed serial interfaces • Multimeters are available for configuration inside the STS

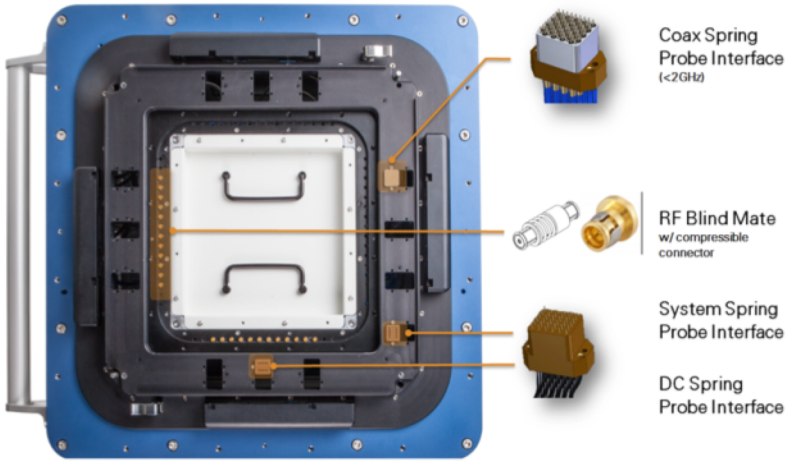


Figure 8. *The STS I/O Interface (Top View)*

STS Device Interfacing

The tester I/O interface at the top of the STS enclosure provides the common interface to all device interface boards/load boards. Figure 8 shows the various I/O interface resources available. High-speed signals (digital and analog) are exposed at this interface through coaxial spring probe blocks. These high-speed I/O pins are often used for digital protocols such as RFFE and high-speed analog signals such as those used for dynamic power supply testing (DPS/ET). All other general-purpose non-RF signals are exposed through DC spring probe blocks often used to expose PXI SMUs and DC power supplies. The STS RF subsystem shown earlier is exposed through an SMP RF blind mate interface, each side of the DIB locker can support up to 12 RF ports for a total of 48 inside an STS T4. All electrical I/O is mechanically locked to a common STS DIB locker, allowing for rapid tester load board interchange and handler/prober hard dock configurations. Additionally, the STS DIB locker is pneumatically, electrically, or manually operated to ensure a mechanically rigid and repeatable connection. Figure 9 shows an example of an STS T2 mechanically hard docked to a gravity-fed handler.

Figure 9. *The STS T2 Hard Docked to Gravity-Fed Handler*

STS I/O Interface Calibration

All electrical measurement I/O is exposed through the tester I/O interface shown in Figure 8. Test engineers need a solution to provide calibrated signals and measurements at this interface. For RF signals, an RF multiport calibration module is used to perform a full vector and scalar RF calibration. Figure 10 shows the full 48-port version. To have calibrated results at the DUT, users can apply de-embedding corrections from standard S2P files.

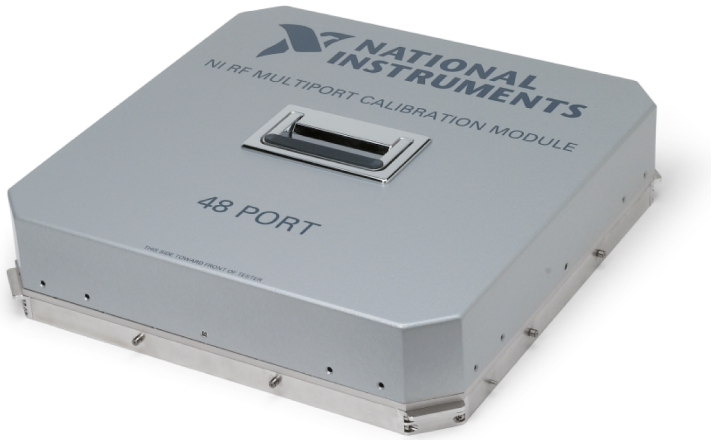


Figure 10. *NI RF Multiport Calibration Module (Vector and Scalar Calibration)*

For non-RF signals on spring probe blocks, a separate system calibration module is used to verify digital and DC signals. Because the STS is very configurable, the digital and DC verification and calibration module is configured to match the spring probe I/O and instrumentation configuration specific to a tester.

Introduction to the STS Software

At the core of the STS software is TestStand ready-to-run test management software designed to help engineers quickly develop, debug, and deploy test programs. TestStand includes many standard features, such as flow control, debugging breakpoints, database logging, and enterprise system connectivity, which are often used in both characterization and production. Specific to the semiconductor test application, the TestStand Semiconductor Module software package adds several features to the TestStand environment including:

- Multisite abstraction
- Pin and channel map abstraction
- DUT-centric programming
- Easy-to-use operator interface
- Test results binning
- STDF reports
- Handler/prober integration

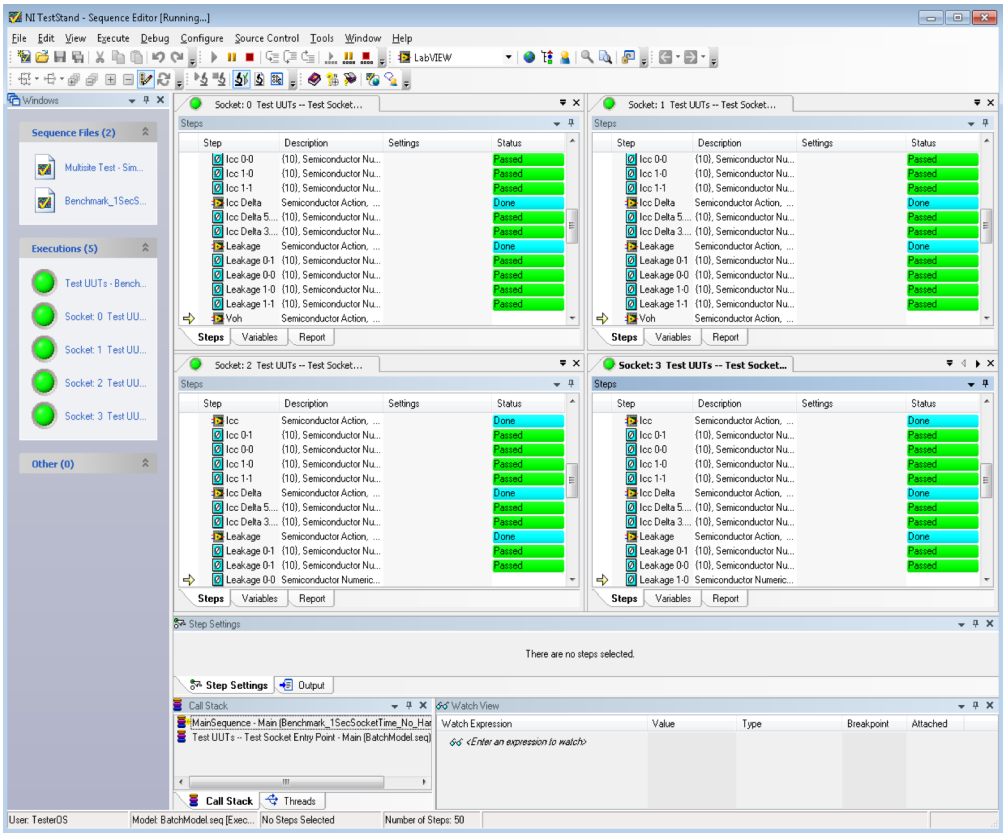


Figure 11. *TestStand With TestStand Semiconductor Module Multisite Debugging*

Multisite and Pin and Channel Map Abstraction

Production test parallelism can be challenging to engineer efficiently and correctly. Ideally, a test program should be written so it is unaware if it is being run single site or octal site or with parallel or shared instrument resources. This is where the multisite and pin map abstraction helps the test engineer to program relative to the DUT rather than the tester I/O pin or instrument channel. The STS pin and channel map abstraction maps the DUT pins to I/O pins and instrumentation resources through a system XML document. During test runs, code modules route the signals all without the test engineer having to know the internal configuration of the tester. This has the benefit that one could write a single program to do preproduction validation on an STS T1 and scale to quad site on an STS T4 with parallel resources without changing the test program. Figure 11 shows an example of a quad site test program in TestStand where a single program is run in four parallel threads. This particular view is the one a test engineer would use to debug and view trace execution. The production test operator wouldn't have such detail as they would be working with an operator interface.

Operator Interface, Binning, and Test Reports

Production operators are not tasked with test program development; their main concerns involve product yield, uptime, and throughput. A consistent and easy-to-use graphical user interface is a critical part to performing their job efficiently. The TestStand Semiconductor Module includes a prebuilt operator interface with built-in station and lot configuration menus that show all the capabilities needed to set up a test program and handler without having to work with the test program development interface. Figure 12 shows the module operator interface performing an octal site test. In addition to station, setup operators have access to test results binning information that provides insight into the tests failing most often. The module supports many report formats such as STDF, which is ubiquitous in the semiconductor production test industry. Reports are generated at lot completion, but mid-lot summaries are also available if needed. Because the operator interface is built on LabVIEW software and is provided

as open source, production test organizations can add customizations such as operator login mechanisms using RFID or bar code scanners.

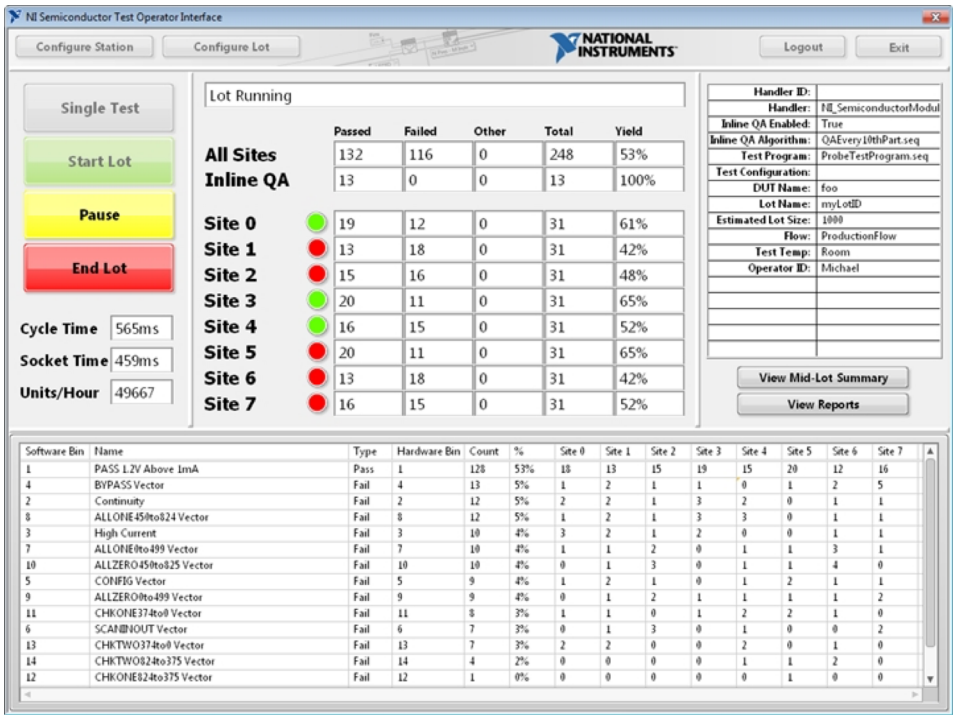


Figure 12. *TestStand Semiconductor Module Operator Interface*

Example Configuration for a RF FEM Test

The STS meets the multiport RF requirements needed for RF FEMs at a significantly lower total cost of ownership than traditional ATEs. Figure 13 shows an instrument mapping block diagram to a single FEM. Because this device has only four RF ports, an STS T2 can easily scale up to quad site test with a 24-port configuration. By using the same PXI modules used in characterization, correlation is significantly simplified. Using STS software abstraction, moving from single site to quad site is seamless as production capacity load increases.

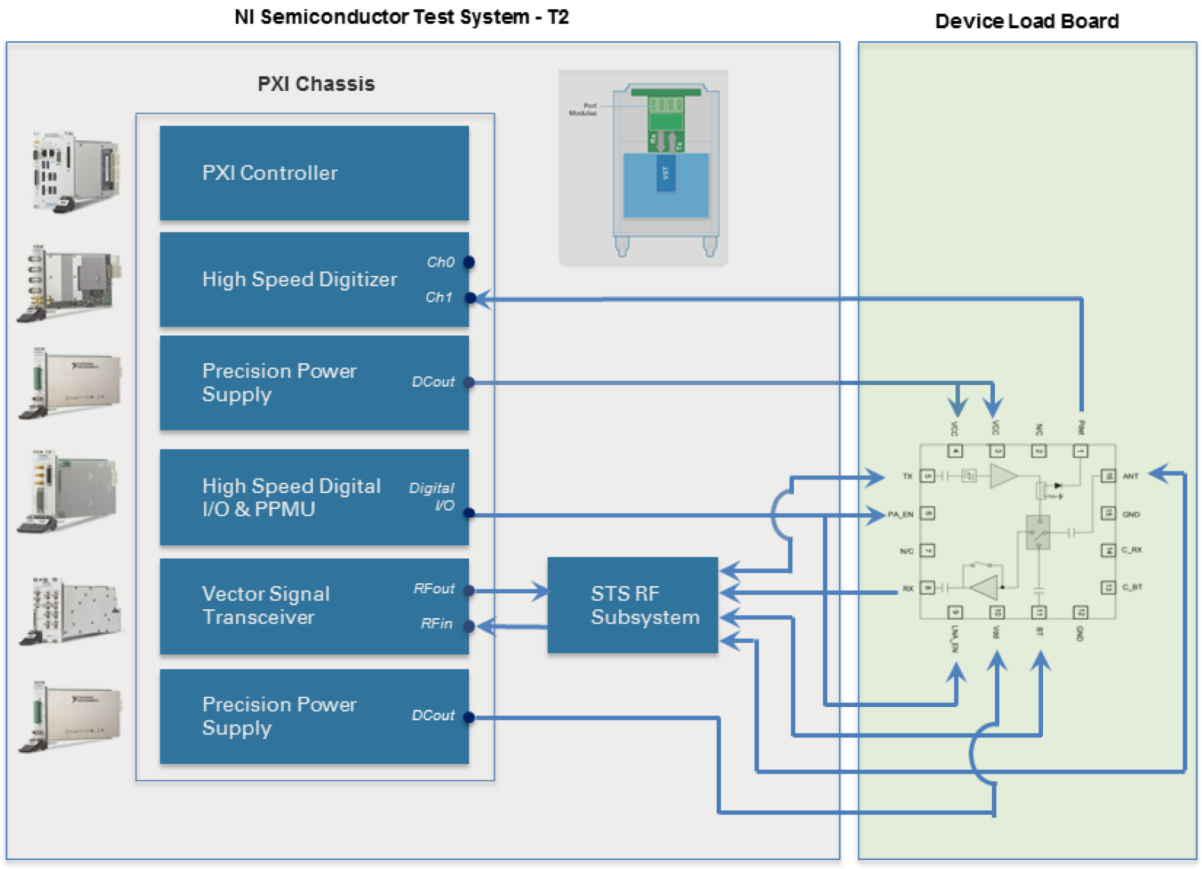


Figure 13. *The STS Configured for Single-Site FEM Test*

Summary

With the modern mobile device revolution, semiconductor suppliers are challenged to increase capability, integration, and performance while reducing time to market. Test needs a new approach based on an open, flexible platform at significantly lower cost. NI is bridging this gap by building on the stability and capability of the PXI platform to deliver off-the-shelf modular technology to both the characterization and production engineer. The STS builds on the industry-standard PXI platform to deliver semiconductor production test cell-specific features that lower the cost of test and shorten time to market for RFIC products.